Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHIGENOBU MAEDA

Appeal No. 2003-1310
Application No. 09/761,738[1]

HEARD: JANUARY 20, 2004

Before FLEMING, BARRY, and SAADAT, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL AND ORDER

This is a decision on appeal from the Examiner's final rejection of claims 21-24. Claims 1-20 have been cancelled.

We affirm.

BACKGROUND

Appellant's invention is directed to a manufacturing method of semiconductor wafers for improving adaptability to the

[1] Application for patent filed January 18, 2001, which is a divisional of the Application No. 09/349,514, filed July 9, 1999, now U.S. Patent No. 6,231,673, which claims the foreign filing priority benefit under 35 U.S.C. § 119 of Japanese Application No. P11-14303, filed January 22, 1999.

expansion or reduction of the production scale. Recent development of the semiconductor manufacturing techniques allows integrating larger number of circuit elements into a single semiconductor chip, trailed by combining various circuit components, also known as "micro cell" or "Intellectual Property (IP)." Each IP is composed of a plurality of circuit elements and performs a certain function (specification, page 2, line 22 through page 3, line 2). A mask pattern of each IP is generated and transferred to a predetermined position of the semiconductor chip based on an overall layout information (specification, page 34). As depicted in Figure 39, superposition marks 132 are patterned around an IP mask pattern 131 on a mask 130, which are used to properly position each of the IP patterns 131 (specification, page 35).

Representative independent claim 21 is reproduced as follows:

> 21. A method of manufacturing a semiconductor device for building a circuit composed of combined plural intellectual properties into a semiconductor chip, comprising:
>
> arranging each mask pattern of said plural intellectual properties for a layout pattern.

The Examiner relies on the following prior art reference:

Krolikowsky et al. (Krolikowsky) 3,760,384 Sep. 18, 1973

Claims 21-24 stand rejected under the second paragraph of 35 U.S.C. § 112 as being indefinite.

Claims 21-24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Krolikowsky.

Rather than reiterate the viewpoints of the Examiner and Appellant regarding the rejections, we make reference to the answer (Paper No. 11, mailed August 30, 2002) for the Examiner's reasoning and to the appeal brief (Paper No. 10, filed July 22, 2002) and the reply brief (Paper No. 13, filed October 24, 2002) for Appellant's arguments thereagainst.

OPINION

With respect to the rejection of the claims under the second paragraph of 35 U.S.C. § 112, the Examiner questions the clarity and the meaning of the term "intellectual property" as "circuit components" (answer, page 3). Appellant argues that the use of the term "intellectual property" as predefined circuits that can be formed on a semiconductor wafer as a component of a larger operational circuit are known in the industry (brief, page 4). Appellant further provides copies of web-page printouts to support the use of the term "intellectual property" in this context as used in semiconductor manufacturing art (brief, Appendix II).

In response, the Examiner indicates that the accepted meaning of the term "intellectual property" is "intangible creation of the human intellect that are [is] protected by law" which indicates that the claimed term is indefinite (answer, page 4). The Examiner further argues that because the term "intellectual property" may be used to mean different things, the scope of the claims is indefinite (id.).

Analysis of 35 U.S.C. § 112, second paragraph, should begin with the determination of whether claims set out and circumscribe the particular area with a reasonable degree of precision and particularity; it is here where definiteness of the language must be analyzed, not in a vacuum, but always in light of teachings of the disclosure as it would be interpreted by one possessing ordinary skill in the art. In re Johnson, 558 F.2d 1008, 1015, 194 USPQ 187, 193 (CCPA 1977), citing In re Moore, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (1971). "The legal standard for definiteness is whether a claim reasonably apprises those of skill in the art of its scope." In re Warmerdam, 33 F.3d 1354, 1361, 31 USPQ2d 1754, 1759 (Fed. Cir. 1994). Furthermore, it is settled that a claim which is of such breadth that it reads on subject matter disclosed in the prior art is rejected under 35 U.S.C. § 102 rather than under 35 U.S.C. § 112, second paragraph.

See In re Hyatt, 708 F.2d 712, 715, 218 USPQ 195, 197 (Fed. Cir. 1983) citing In re Borkowski, 422 F.2d 904, 909, 164 USPQ 642, 645-46 (CCPA 1970).

Upon a careful review of the claim language and the specification, we find that the claimed term "intellectual property" clearly refers to a large number of circuit elements integrated into a single semiconductor chip as a component of a larger functional circuit. It is clear from the specification as a whole, and page 34 specifically, that a mask pattern of each IP constituting the entire circuitry is generated and transferred to a predetermined position of the semiconductor chip. The specification on page 35 also provides for an arrangement for positioning the mask patterns by using superposition marks around mask patterns that are to be placed in their corresponding positions on the semiconductor chip where the pattern in to be transferred.

In view of the above and in light of the specification as a whole, we find that the term "intellectual property" is sufficiently defined and would reasonably apprise those skilled in the art of the scope of this limitation. Accordingly, we will not sustain the rejection of claims 21-24 under the second paragraph of 35 U.S.C. § 112.

With regard to the rejection of the claims under 35 U.S.C. § 102, Appellant argues that Krolikowsky discloses a method of fabricating a field effect transistor (FET) memory chip by using separate masks to define and form different regions of the FET (brief, page 6 and reply brief, page 4). Appellant further asserts that these masks are mask patterns of a discrete electronic component and not that of a plurality of intellectual properties that may be arranged for a layout pattern (brief, page 6 and reply brief, page 5).

The Examiner responds to Appellant's arguments by stating that claim 21 merely requires arranging mask patterns of a plurality of functional circuits where each includes a plurality of circuit elements (answer, page 5). Relying on the breadth of claim 21, the Examiner asserts that Krolikowsky's method of fabricating a field effect transistor discloses and reads on the claimed method of arranging mask patterns (id.). The Examiner argues that the transistor is fabricated by using mask patterns prepared for plural circuit elements such as a gate electrode, source and drain performing certain functions (id.).

As a general principle, a rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference.

In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994), citing In re Spada, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990). The inquiry as to whether a reference anticipates a claim must focus on what subject matter is encompassed by the claim and what subject matter is described by the reference. As set forth by the court in Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983), it is only necessary for the claims to "'read on' something disclosed in the reference, i.e., all limitations of the claim are found in the reference, or 'fully met' by it."

After reviewing Krolikowsky, we find that the Examiner presents sufficient evidentiary support to establish a prima facie case of anticipation. Krolikowski relates to memory array and its method of manufacturing for laying out a very dense FET array on a small chip area having small spacing and dimension rules (abstract). In Figures 9A-9D, Krolikowsky shows the steps for arranging exemplary mask patterns related to the N+ regions (source and drain regions), contact holes, gate and the metallization pattern of a FET as a part of the memory array (col. 11, lines 20-28). In particular, Krolikowsky shows that at each step, the corresponding alignment mark is matched with the previous ones to position different circuit elements according to

their layout pattern (col. 11, lines 29-46). Therefore, we do not agree with Appellant (brief, page 6) that Krolikowsky's mask patterns relate to portions of a discrete component (i.e., the FET) and do not provide mask patterns of a plurality of intellectual properties. In that regard, as a plurality of circuit elements are required to form an intellectual property, the source/drain regions, the gate and the metallization of different components of a memory array may be reasonably considered as the circuit elements that are formed using different mask patterns and are arranged according to a layout pattern. Thus, the Examiner has properly corresponded the mask patterns of the memory array as the claimed mask patterns of an intellectual property which is formed of different elements of the transistors, contacts and the conducting connections in the memory array according to its specific layout. In fact, similar to Appellant's method of arranging the mask patterns, Krolikowsky uses alignment marks to arrange the mask patterns of different circuit elements to form the entire layout pattern corresponding to that of a memory array.

In view of the analysis above, we find that the examiner has met the burden of providing a prima facie case of anticipation as Krolikowsky teaches a plurality of circuit elements or components

of a larger operational circuit by arranging different mask patterns for the layout pattern, as recited in Appellant's claim 21. Accordingly, we affirm the rejection of claim 21 as well as claims 22-24, which are grouped by Appellant (brief, page 4) as standing or falling together with claim 21, under 35 U.S.C. § 102 over Krolikowsky.

CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 21-24 under the second paragraph of 35 U.S.C. § 112 is reversed but is affirmed with respect to the rejecting the claims under 35 U.S.C. § 102.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

MICHAEL R. FLEMING)
Administrative Patent Judge)
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) BOARD OF PATENT
LANCE LEONARD BARRY) APPEALS
Administrative Patent Judge) AND
) INTERFERENCES
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MAHSHID D. SAADAT)
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